

**FIG. 1**

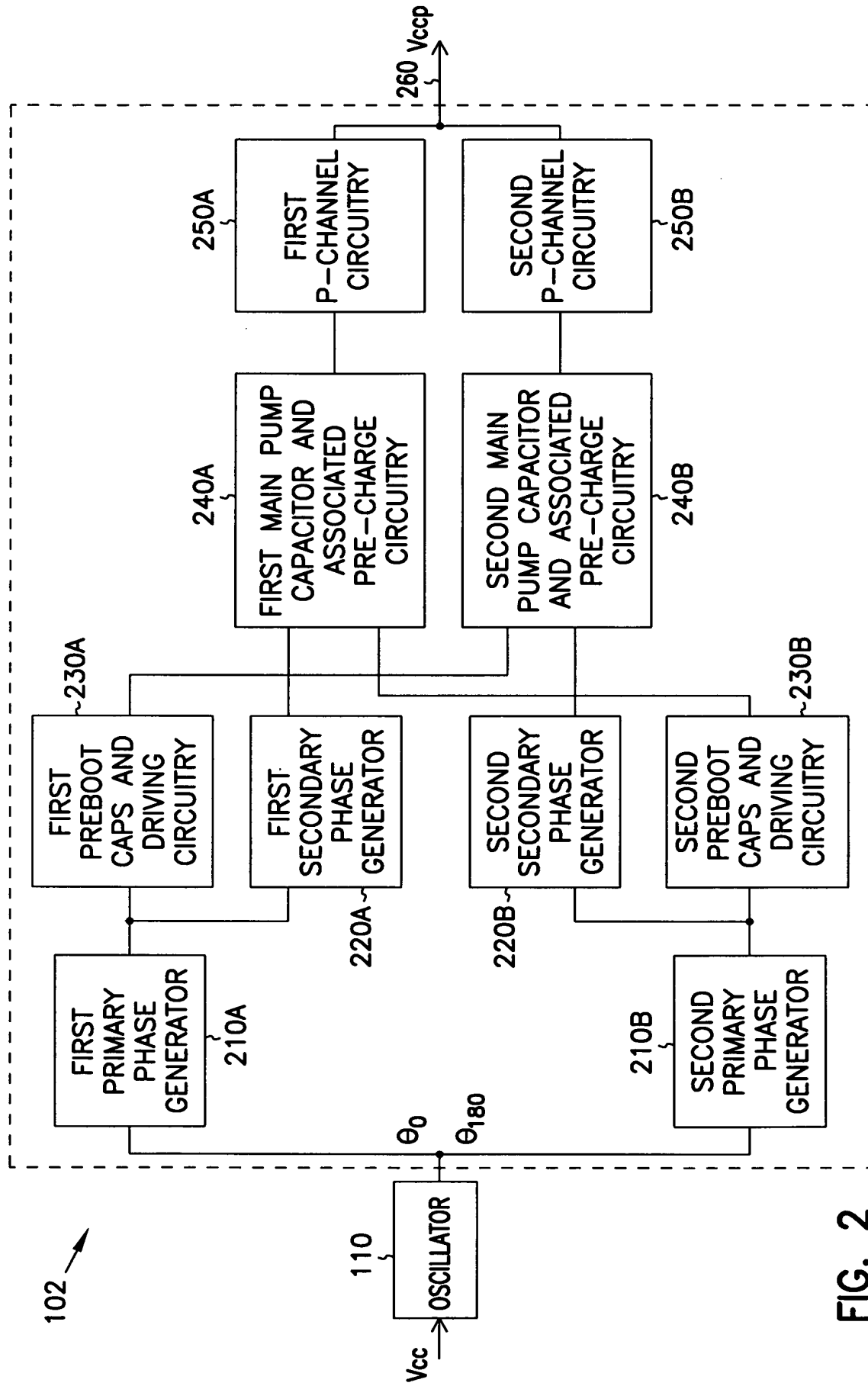
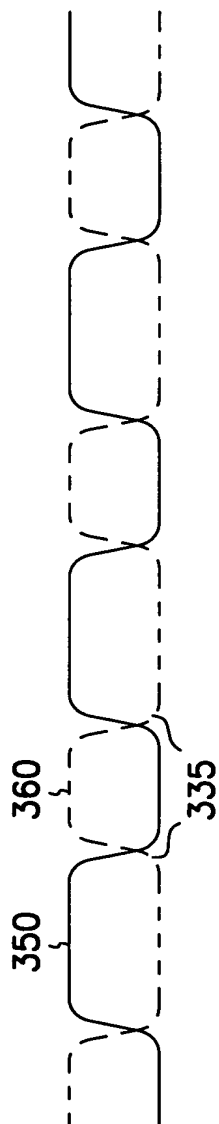
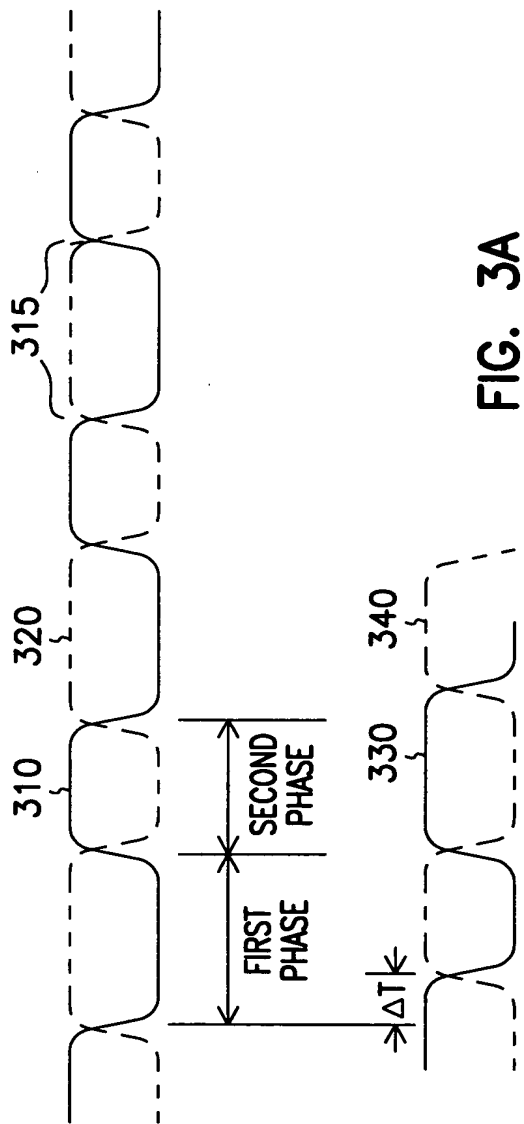


FIG. 2



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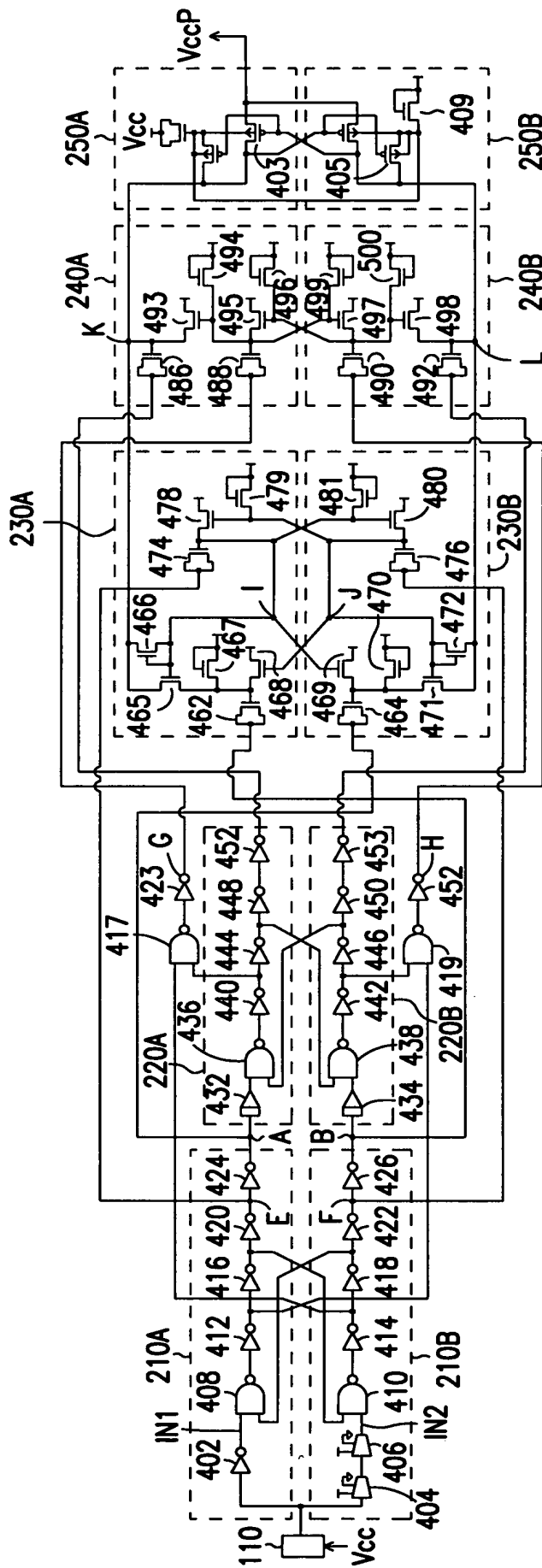


FIG. 4

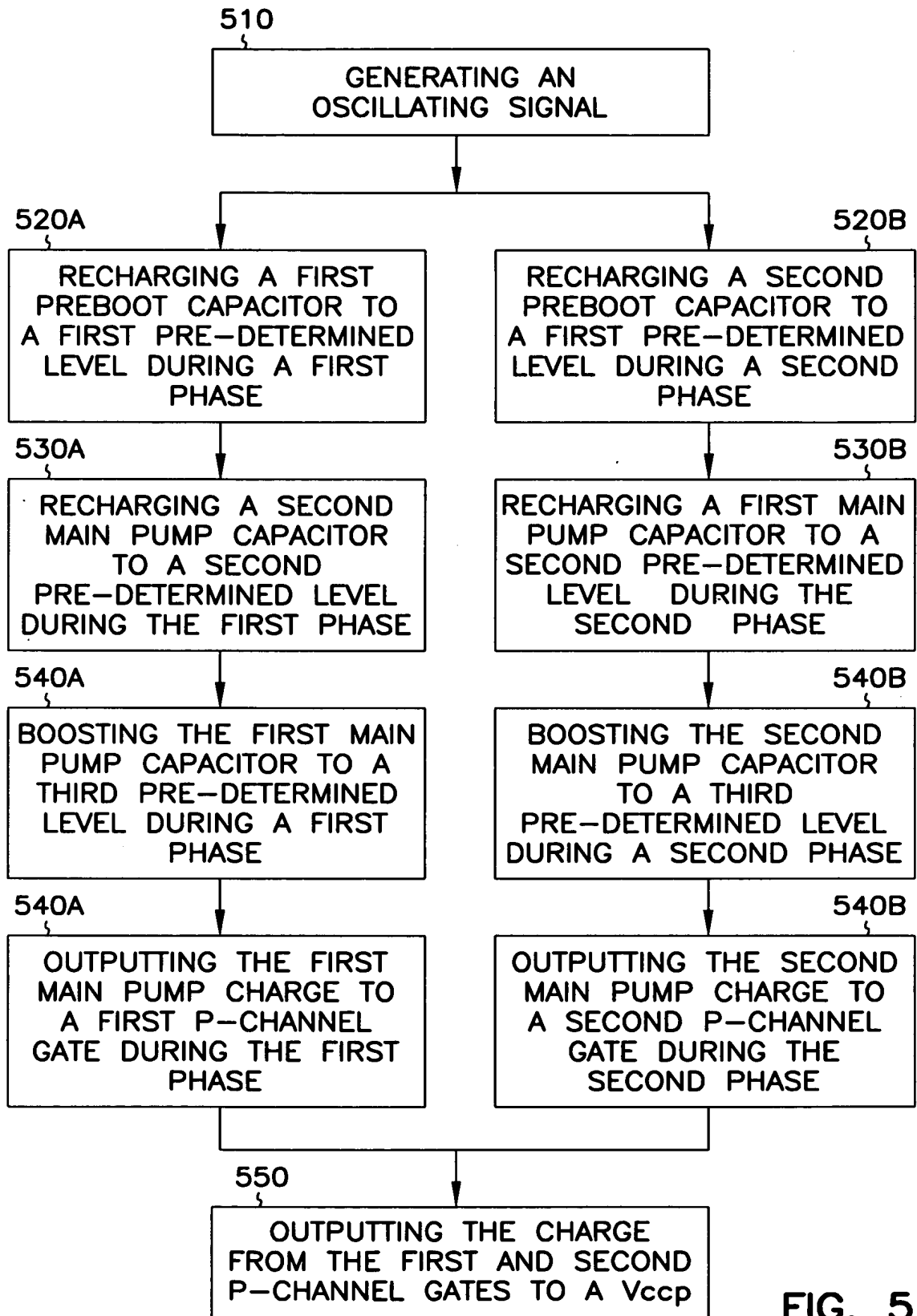


FIG. 5

Timing diagram showing eight digital signals (A-H) over 40 nanoseconds. The signals are labeled A through H, with corresponding device identifiers 610A, 610B, 620A, 620B, 630A, 630B, 640A, and 640B. The signals show various logic transitions and pulses. A vertical scale bar on the left indicates  $V_{CC} = 1.0$  Volts.

**FIG. 6A**

**FIG. 6B**

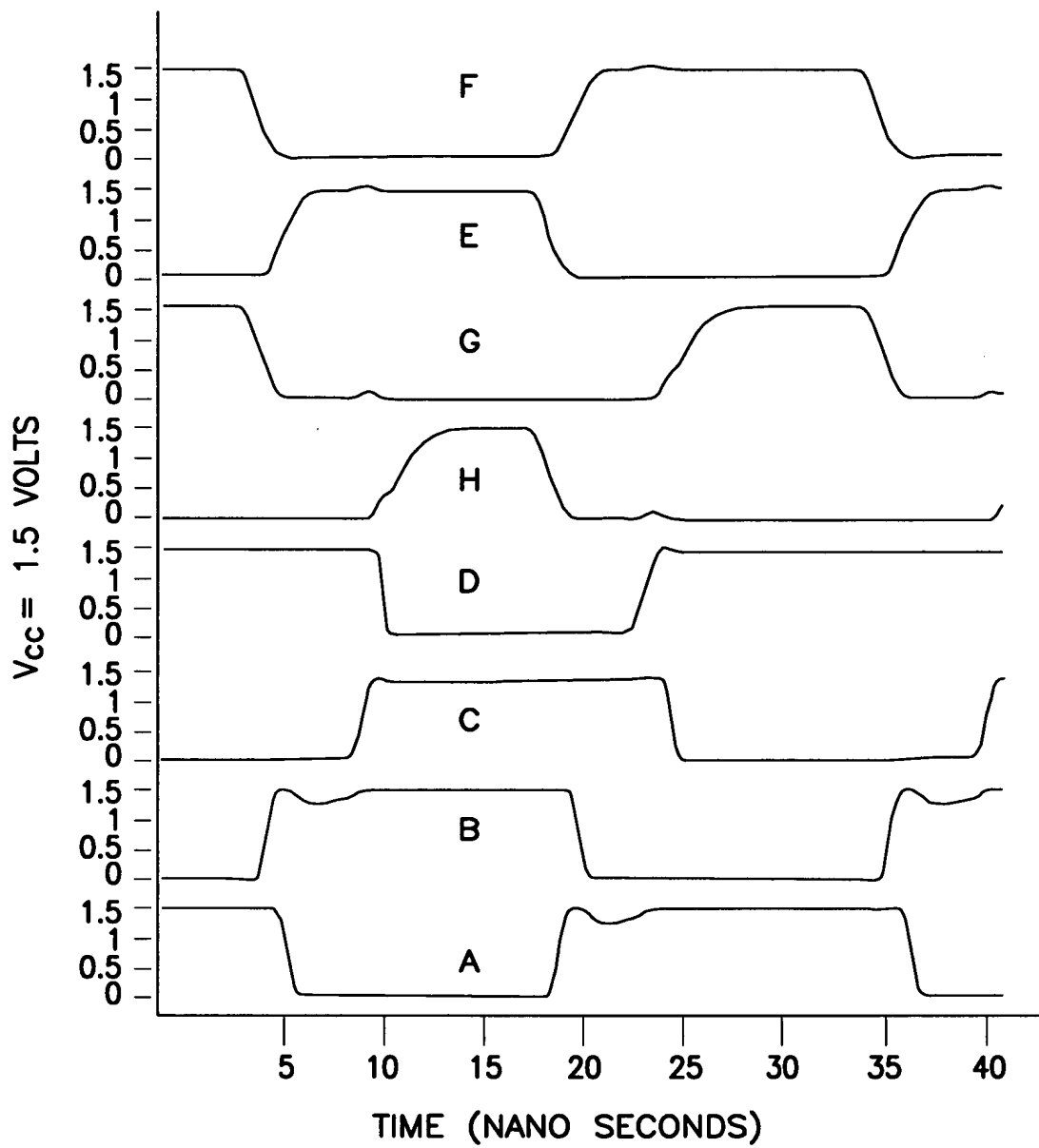


FIG. 7A



The diagram shows five digital signals (A, H, J, K, L) over a 40 ns period. The vertical axis is labeled  $V_{CC} = 1.5 \text{ VOLTS}$  and ranges from 0 to 3. Signal A is a square wave between 0 and 1.5V. Signal H is a square wave between 1.5V and 2.5V. Signal J is a square wave between 1.5V and 2.5V. Signal K is a square wave between 1.5V and 3.0V. Signal L is a square wave between 1.5V and 3.0V.

**FIG. 7B**

**FIG. 8A**

000000 000000 000000

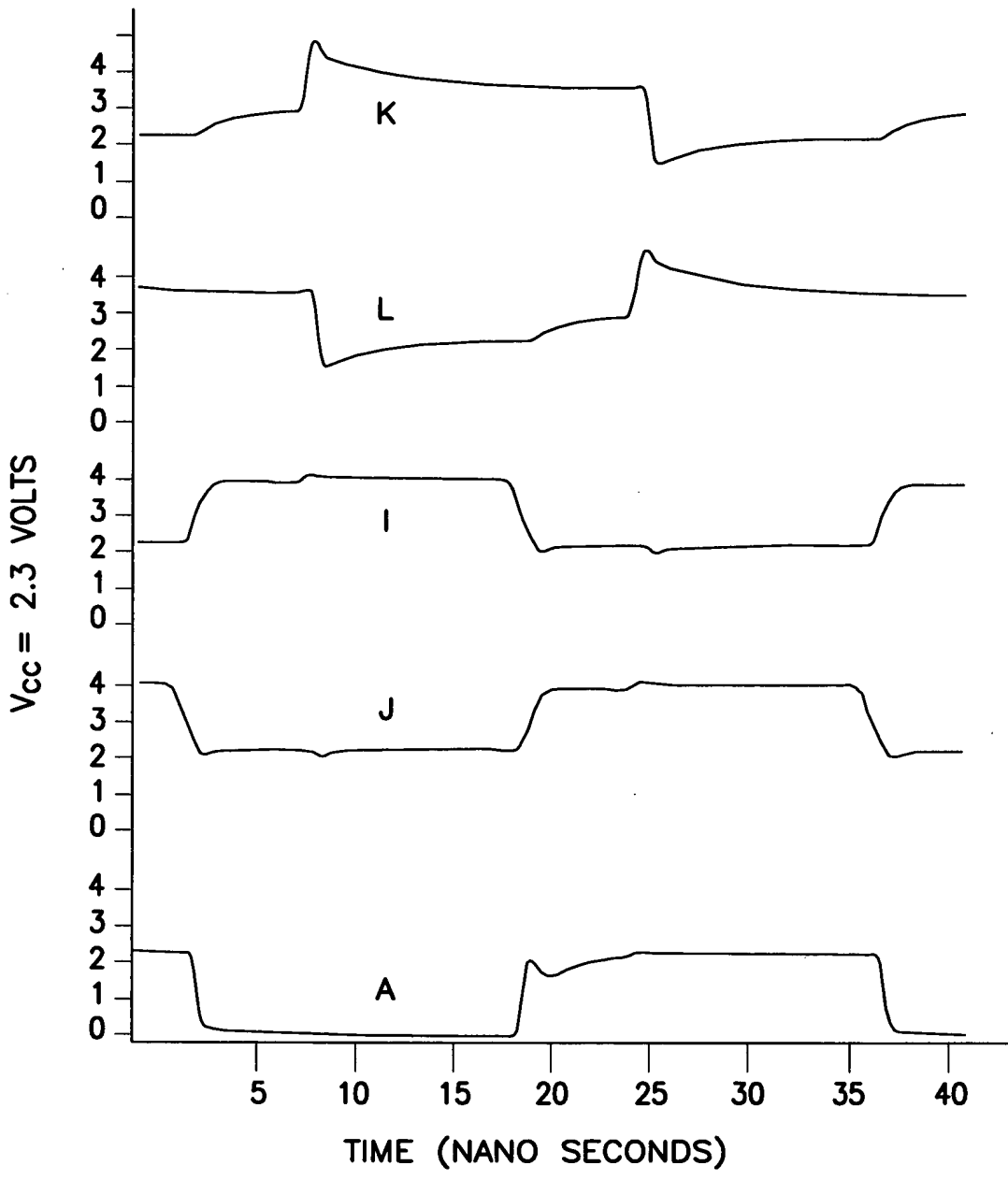


FIG. 8B

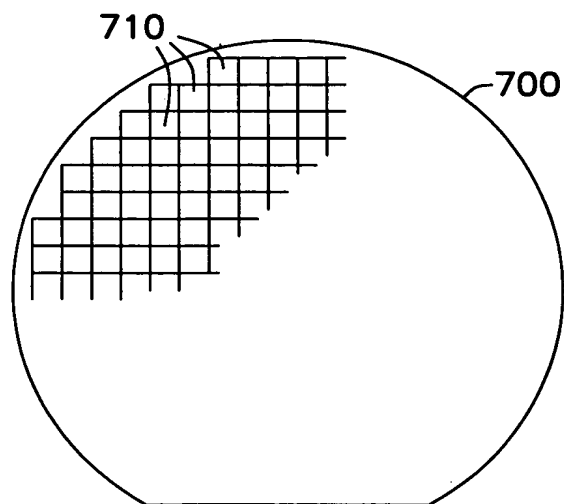


FIG. 9

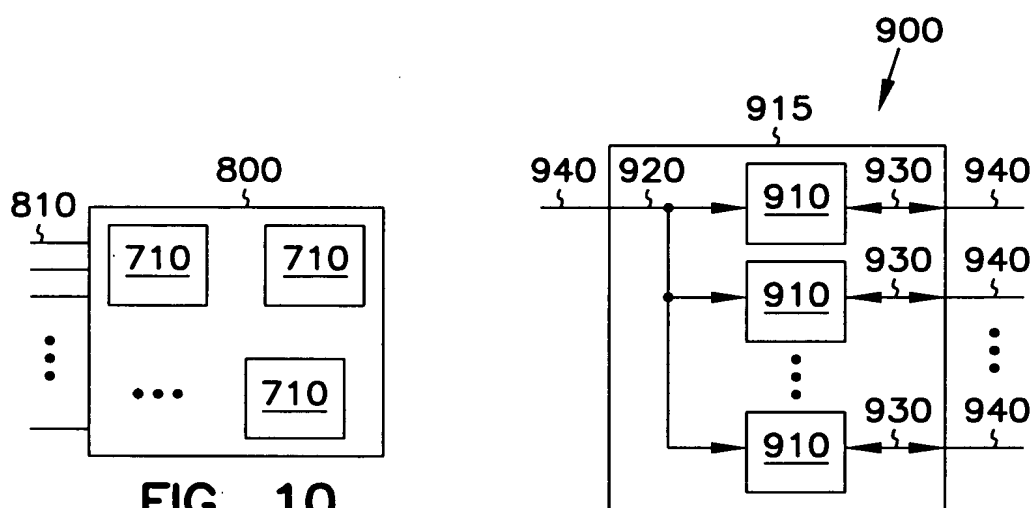


FIG. 10

FIG. 11

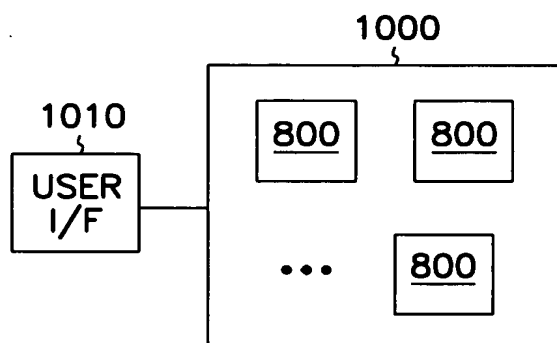


FIG. 12

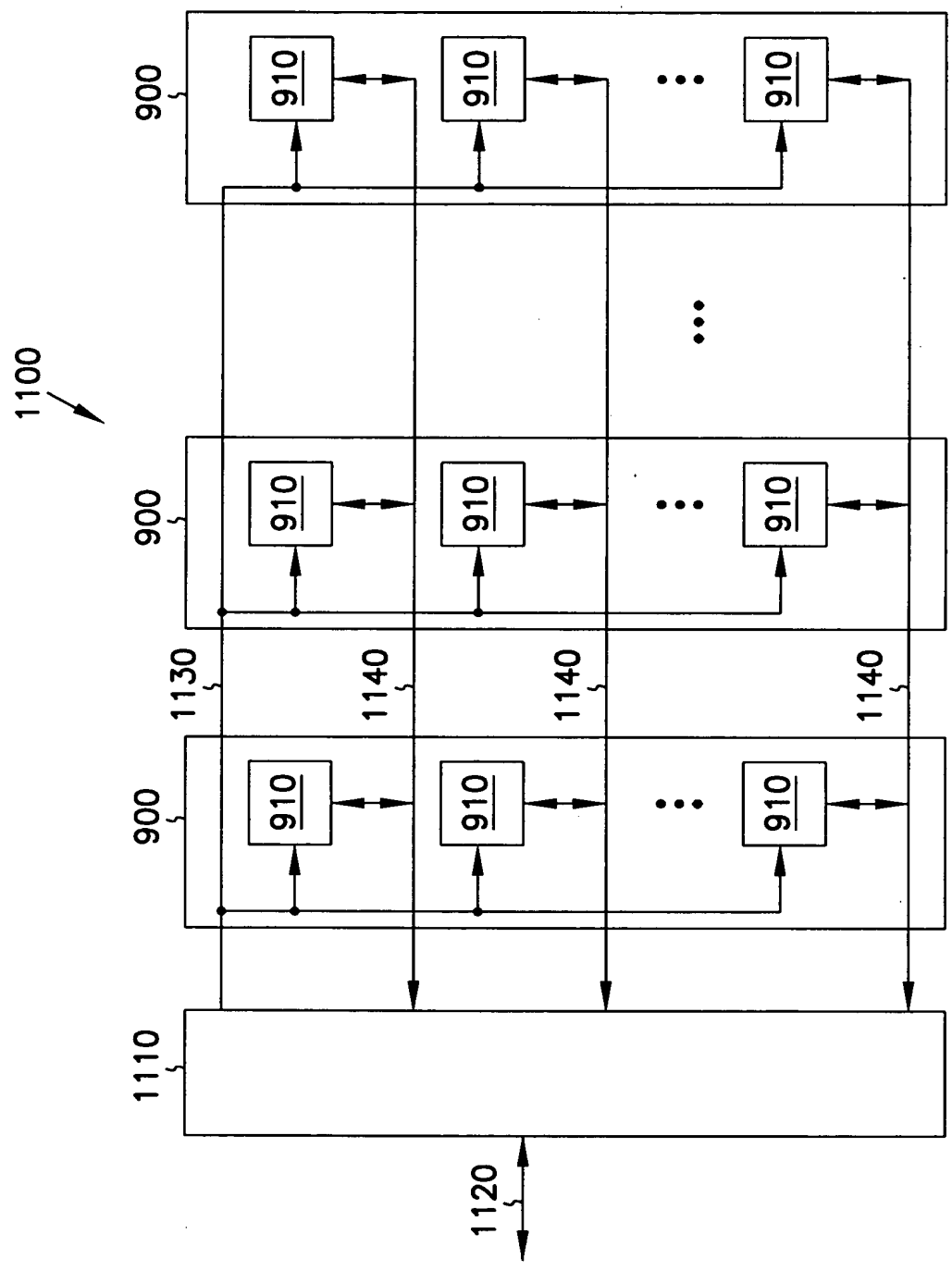


FIG. 13

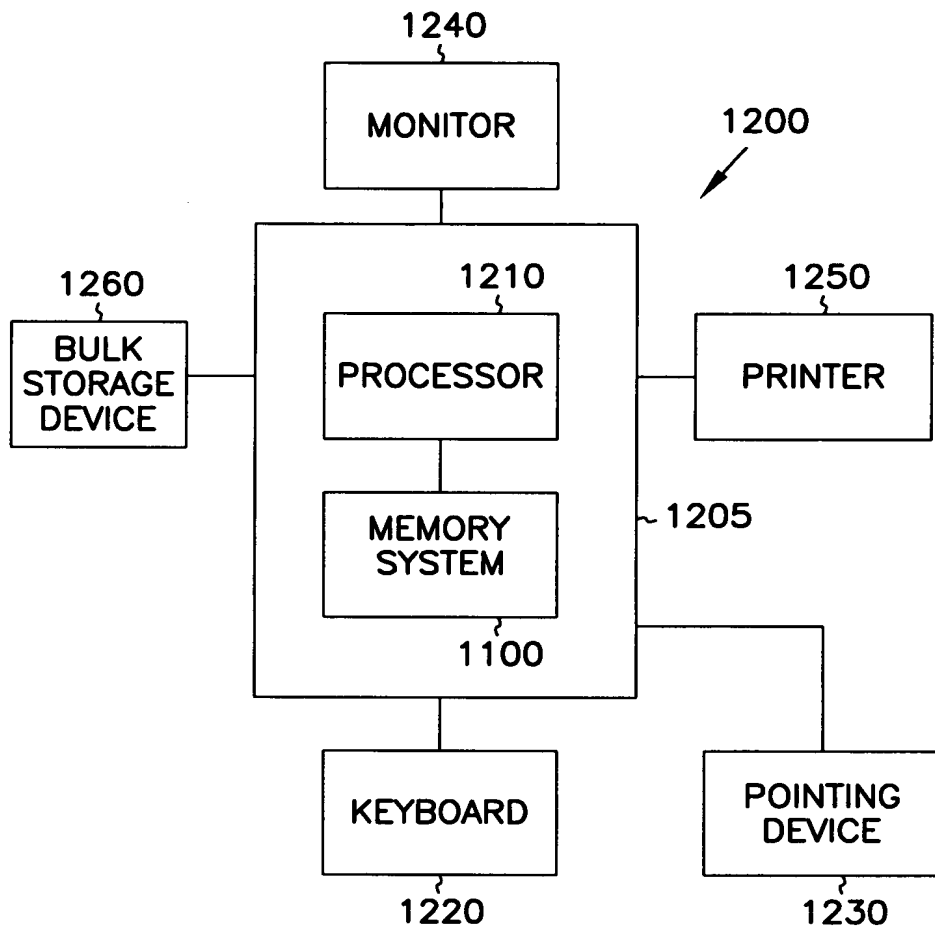


FIG. 14